US-PAT-NO: 6374332

DOCUMENT-IDENTIFIER: US 6374332 B1

TITLE: Cache control system for performing multiple outstanding ownership requests

DATE-ISSUED: April 16, 2002

US-CL-CURRENT: 711/145, 711/150 , 711/151

APPL-NO: 09/ 409756

DATE FILED: September 30, 1999

PARENT-CASE:

CROSS-REFERENCE TO OTHER APPLICATIONS AND ISSUED PATENT

The following co-pending applications of common assignee contain some common disclosure:

"A Directory-Based Cache Coherency System", filed Nov. 5, 1997, Ser. No. 08/965,004, incorporated herein by reference in its entirety;

"Message Flow Protocol for Avoiding Deadlocks", U.S. Pat. No. 6,014,709, issued Jan. 11, 2001, incorporated herein by reference in its entirety;

"High-Speed Memory Storage Unit for a Multiprocessor System Having
Integrated Directory and Data Storage Subsystems", filed Dec. 31, 1997, Ser.
No. 09/001,588, incorporated herein by reference in its entirety; and

"Directory-Based Cache Coherency System Supporting Multiple Instruction
Processor and Input/Output Caches", filed Dec. 31, 1997, Ser. No. 09/001,598,
incorporated herein by reference in its entirety; and

"Directory-Based Cache Coherency System Supporting Multiple Instruction
Processor and Input/Output Caches", a Divisional of Ser. No. 091001,598, filed
Aug. 24, 2000, Ser. No. 09/645,233, incorporated herein by reference in its
entirety.

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Detailed Description Text - DETX (35):

From the above discussion, it is apparent that if a large number of requests
are being processed across the MI Interfaces, the necessity to request
exclusive ownership from the MSU may substantially increase the time required
to perform a write operation. The current invention minimizes the time
required to obtain exclusive ownership by prefetching ownership

before a write request is actually being processed.

Detailed Description Text - DETX (48):

Before the modified data is presented to the SLC, it is temporarily stored in Write Buffer Logic 434. Write Buffer Logic is capable of storing up to eight write requests at once. The data stored within the Write Buffer Logic need not be written to the SLC immediately. That is, generally the Processing Logic 402 may continue executing instructions even though the write data has not been written to the SLC. Processing Logic 402 is only required to wait for the completion of a write operation within the SLC in those situations in which a read operation is requesting access to the same addressable memory location as a pending write request. To detect this situation, the read request on Line 410 is provided to Write Buffer Logic 434, Write Request 2 Logic 438, and Write Request 1 Logic 454 to be compared against all pending write addresses. The conflict is indicated using signals on Lines 462 and 468, respectively. If a conflict is detected, the Processing Logic 402 must wait for the write operation to the SLC to complete so that the IP is guaranteed to receive updated data.